Circuit for Detecting Abnormal Operation of Memory and Integrated Circuit and Method for Detecting Abnormal Operation

Background of the Invention

1. Field of the Invention

The present invention relates to a technique of detecting an abnormal operation of memory built in an integrated circuit and the like of a micro-computer and the like with regard to an access speed and the like.

2. Description of the Related Art

A flash memory is built in some integrated circuits of micro-computers and the like. A control circuit for rewriting and erasing data is added to the integrated circuits in which a memory is built, replacing a mask read only memory with a flash memory and the like. In this conventional integrated circuit, a method for checking the reliability of the written data continuously does not exist.

In the integrated circuits in which a flash memory and the like is built, however, the written data sometimes changes due to a write-in disturbance in rewriting data, a read disturbance in reading out data, a data retention or the like. Or even though the data does not change, the period of time from inputting an address to outputting data, that is, the access time, of the memory sometimes becomes significantly long. If the access time becomes long, the data-outputting cannot keep up with the operation speed of the integrated circuit of the micro-computer and the like. As a result, an error is to occur in the integrated circuit. Especially in the case of using a flash memory for storing an operation program in a micro-computer and the like, the

micro-computer cannot operate normally even when the data output wrongly from the flash memory by only one bit. Therefore, a high cost is needed to ensure the reliability of a memory for storing a program.

In order to correct the error of the output from the memory, using an error correction code (hereafter, referred to as the "ECC") may be considered. In this case, however, a parity bit for correcting is needed as well as a bit for data. And in some cases, a storage capacity is to be needed 1.5 times as much as the program capacity to be actually used. This makes the chip size increase and the cost high. Moreover, the ECC cannot correct the error of data with two bits or more in a single address.

Summary of the Invention

The present invention has been achieved in view of aforementioned problems. The object of the present invention is to provide novel and improved circuit for detecting an abnormal operation of memory, integrated circuit including the same and a method for detecting an abnormal operation, in order to detect an abnormal operation of memory before an error occurs in the integrated circuit of a micro-computer and the like due to the data wrongly output from the memory and to enhance the reliability of integrated circuit.

In the aspect of the present invention to achieve the above object, there is provided a circuit for detecting an abnormal operation of memory comprising: a delay circuit for delaying an output data of the memory for a predetermined period of time and for outputting this data as a delay data; and a comparison circuit for outputting an incoincidence signal in case that the output data of the memory and the delay data are not coincident

with each other after compared.

Brief Description of the Drawings

The above and other features of the invention and the concomitant advantages will be better understood and appreciated by persons skilled in the field to which the invention pertains in view of the following description given in conjunction with the accompanying drawings which illustrate preferred embodiments.

Fig. 1 is a block circuit diagram showing the structure of the first embodiment of the present invention.

Fig. 2 is a timing chart in a normal state of the data signal output from a flash memory in the first embodiment.

Fig. 3 is a timing chart when an abnormality is detected halfway in the data signal output from the flash memory in the first embodiment.

Fig. 4 is a block circuit diagram showing the structure of the second embodiment of the present invention.

Fig. 5 is a timing chart when an abnormality is detected halfway in the data signal output from the flash memory in the second embodiment.

Detailed Description of the Preferred Embodiments

Hereinafter, the preferred embodiment of the present invention will be described in reference to the accompanying drawings. Same reference numerals are attached to components having same functions in following description and the accompanying drawings, and a description thereof is omitted.

(First Embodiment)

Fig. 1 is a block circuit diagram showing the structure of

the first embodiment of the present invention. An address signal output 122 from a CPU 100 is input to an address input terminal of a flash memory 101. Then the data to be stored in the input address in the flash memory 101 is respectively input as a data signal 123 to a data input terminal of the CPU 100, to an input terminal D of a first data latch 103 and to an input terminal of a delay circuit 102. The data signal 123 input to the delay circuit 102 is output as a delay circuit output 124 delayed for a predetermined period of time, and is input to the input terminal of a second data latch 104.

And then a data latch signal 125 of the first data latch 103 is input to one input terminal A of a comparator 106. The data output of the second data latch 104, that is, a delay data latch signal 126 is input to the other input terminal B of the comparator 106.

On the other hand, a latch signal 121 from the CPU 100 is respectively input to a latch signal input terminal G of the first data latch 103, to a latch signal input terminal G of the second data latch 104 and to an output control terminal OE (Outlet Enable) of the comparator 106. Each of the data latch signal 125 and the delay data latch signal 126 holds the latched value in rising of the latch signal 121 in an H section of the latch signal 121. On the other hand, the data latch signal 125 and the delay data latch signal 126 output the data signal 123 and the delay circuit output 124 at that time through in an L section of the latch signal 121.

At each timing of the rising of latch signal 121 to be input to the output control terminal OE, the comparator 106 outputs a logical signal "L" if the signal at the input terminal A equals to the one at the input terminal B, and outputs a logical signal "H"

as an incoincidence signal 127 if the signal at the input terminal A does not equal to the one at the input terminal B. Then the incoincidence signal 127 from the comparator 106 is input to an input terminal CK of a D-FF 107. A power source 128 from a power source VDD 110 is connected to an input terminal D of the D-FF 107. And then an abnormality detecting signal 130 turning into "H" state in detecting an abnormality is output from an output terminal Q of the D-FF 107, which is connected to an external output terminal 108. Also, a reset signal 129 from the external output terminal 109 is connected to a reset input terminal R of the D-FF 107. And then when the reset signal 129 is input from the external output terminal, the abnormality detecting signal 130 returns to "L" state (Fig. 1).

Next, the operation of the first embodiment will be explained in reference to Figs. 1-3. Fig. 2 is a timing chart in a normal state of the data signal output from a flash memory in the first embodiment. Fig. 3 is a timing chart when an abnormality is detected halfway in the data signal output from the flash memory in the first embodiment.

The flash memory 101 outputs the data signal 123 at a timing t_1 after a certain period of time (access time; $(t_1 - t_0)$), receiving the address signal 122 from the CPU 100 with the starting point set at "t_0". The CPU 100 downloads the data of the data signal 123 at a timing t_3 at which the latch signal 121 turns into "H" state, and processes the data in the CPU 100, based on a predetermined program (Fig. 2).

The data signal 123 is delayed for a period of time $(t_2 - t_1)$ in the delay circuit 102 and is output as the delay circuit output 124. The data signal 123 and the delay circuit output 124 are respectively compared in the comparator 106 via the first data

latch 103 and the second data latch 104. If they are coincide with each other at the timing t_3 at which the latch signal 121 rises to turn into "H" state, the incoincidence signal 127 remains "L" state (Fig. 2).

However, if the access time of the flash memory 101 is delayed and the output of the data signal 125 misses a timing t_5 without outputting at a timing t_4 after receiving the address signal 122, the delay circuit 102 cannot output the data by a timing t_6 at which the latch signal 121 rises to "H" state and the comparator 106 judges to be incoincident, to turn the incoincidence signal 127 into "H" state (Figs. 1 and 3).

If there is a rising edge at which the incoincidence signal 127 turns into "H" state, the D-FF 107 downloads the "H" data at the input terminal D connected to the power source VDD 110 and an abnormality detecting signal 130 is turned from "L" state into "H" state. Then it is notified to the outside that the output of the external output terminal 108 connected to the output terminal Q of the D-FF 107 turns from "L" state into "H" state and that the access time of the flash memory has changed (been delayed), in other words, the abnormal operation of the flash memory 101 (Figs. 1 and 3).

If the abnormal operation is detected in the flash memory 101, some operation may be implemented outside thereof, for example: sounding alarm with sound, image and animation; urging backup; carrying maintenance; and so on. In returning the output from the external output terminal 108 from "H" state into "L" state, the state of the D-FF 107 should be reset by turning the signal to be input into the external input terminal 109 from "L" state into "H" state (Fig. 1).

According to the first embodiment as described above, the

access speed of the data signal is high enough to match the timing to use in the CPU, however, it is monitored whether the incoincidence will occur or not by giving a predetermined period of delay and by comparing the data before and after the delay with each other. In other words, by checking whether the margin for delay is always saved with regard to the timing for the CPU to download the data signal, it can be detected that the access speed in the flash memory begins to become lowered for some reasons when the incoincidence occurs, though there is an enough amount of margin in an initial state. Consequently, we can learn an abnormality before an error occurs in the integrated circuit of the micro-computer and the like in which a flash memory is built operates abnormally due to a wrong data signal with the access speed further lowered.

(Second Embodiment)

Fig. 4 is a block circuit diagram showing the structure of the second embodiment of the present invention. There are some points different from those in the first embodiment: providing an address latch 205; and connecting an output terminal Q of a D-FF 207 connected to the external output terminal 108 in the first embodiment to the interruption control circuit 211 in this second embodiment. Hereafter, an explanation is to be given with regard to the different points while an explanation is to be omitted with regard to the same points as the ones in the first embodiment.

An address signal output 222 from a CPU 200 is connected to a D-latch of the address latch 205 while a latch signal 221 is input to one end of a two-input NAND element 213. The output terminal Q of the D-FF 207 is connected to the interruption control circuit 211 and to an input terminal of an

inverter 214 while an output 231 from the inverter 214 is input to the other end of the two-input NAND element 213. An output 232 (NAND output) from the two-input NAND element 213 is connected to a latch signal input terminal G of the address latch 205. And then a latch output 233 from the address latch 205 is connected to a data bus 212 while a reset signal 229 from the interruption control circuit 211 to a reset input terminal R of the D-FF 207 (Fig. 4).

Next, the operation of the second embodiment will be explained in reference to Figs. 4 and 5. Fig. 5 is a timing chart when an abnormality is detected halfway in the data signal output from the flash memory in the second embodiment.

The explanation of the flow of operation from the beginning until outputting an abnormality detecting signal 230 from the output terminal Q of the D-FF 207 is to be omitted since it is the same as the one in the first embodiment. When the abnormality detecting signal 230 turns into "H" state, it is input to the interruption control circuit 211 as an interruption signal to execute the pre-programmed interruption process in the CPU 200. There are some options as the interruption process, for example, notifying an abnormality, rewriting memory, and so on.

In referring to an address judged to be incoincident during the interruption process, the address latched by the address latch 205 in the rising of the NAND output 232 of the latch signal 221 and of an inversion signal 231 of the abnormality detecting signal 230 remains latched during the period when the abnormality detecting signal 230 is in "H" state. Therefore, the address can be read out via the data bus 212. After finishing the execution of the interruption process, the reset signal 229 is output from the interruption control circuit 211. And then the

D-FF 207 becomes reset, and the abnormality detecting signal 230 returns to "L" state from "H" state (Figs. 4 and 5).

According to the second embodiment as described above, when the margin runs short with regard to the access speed of data, an internal signal in an integrated circuit of micro-computer and the like can be used to cope with this problem as well as outputting a signal to the external output terminal. Also, since the address of the data with the margin thereof run short can be held and can be read out by the CPU, the rewriting of the address data can be automatically executed before an error occurs in the CPU.

In the second embodiment, when the access speed can be recovered with such a process as rewriting the flash memory, since the process from the outside is not needed the reliability of a built-in flash memory can be enhanced, as a result.

Also in the first and second embodiments, the delay time in the delay circuit is fixed. However, the margin of access speed to be judged abnormal can be adjusted by providing the circuit in which the delay time can be adjusted inside the delay circuit. Hereby the yield of product can be enhanced by being capable of considering the unevenness in quality due to the quality of the built-in flash memory.

According to the embodiments as described above, there has been explained by giving an example in which a flash memory is used, however, the memory to be utilized in the present invention is not restricted to this example.

Although the preferred embodiment of the present invention has been described referring to the accompanying drawings, the present invention is not restricted to such examples. It is evident to those skilled in the art that the present

invention may be modified or changed within a technical philosophy thereof and it is understood that naturally these belong to the technical philosophy of the present invention.